

Fig.1

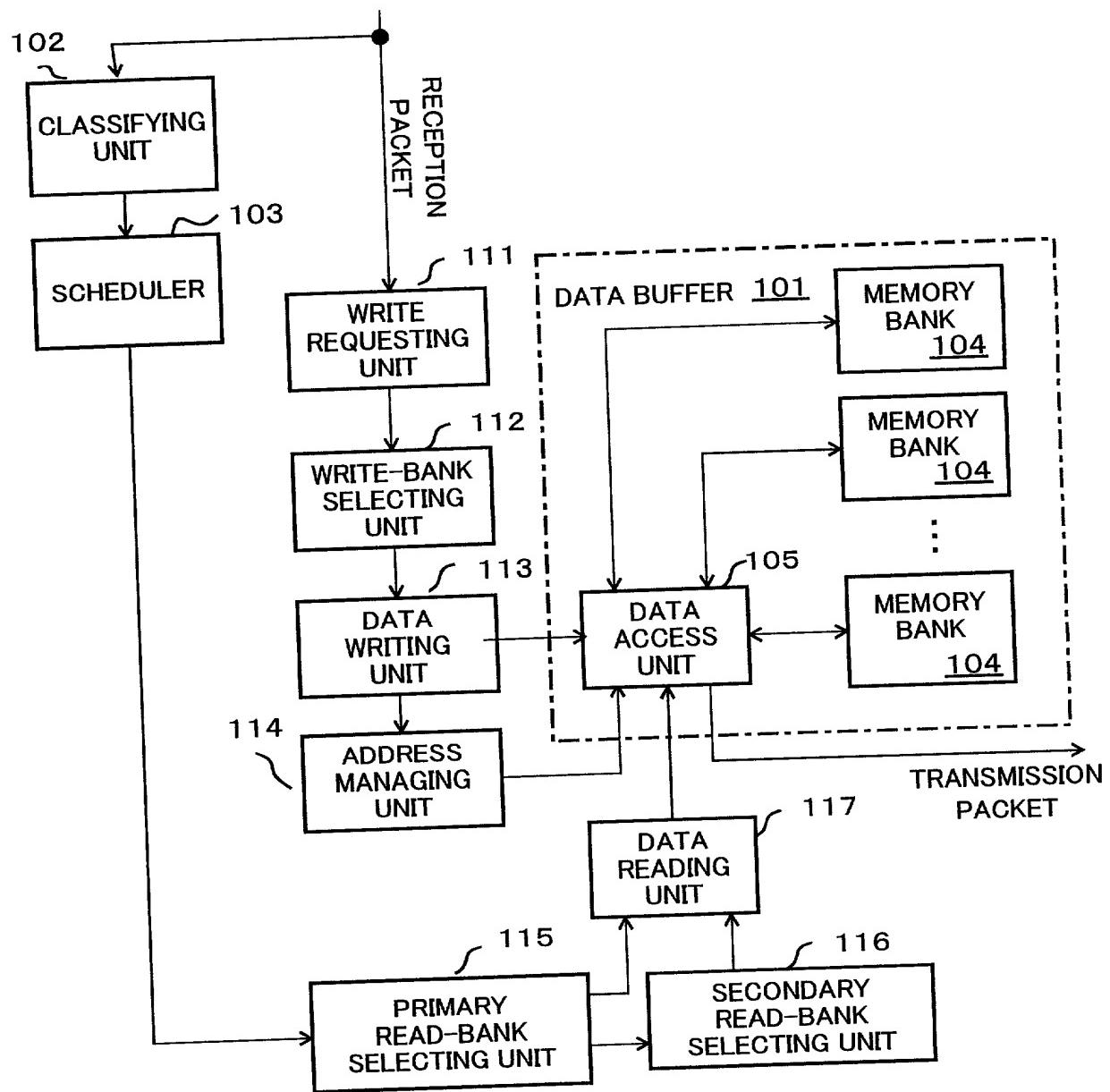


Fig.2

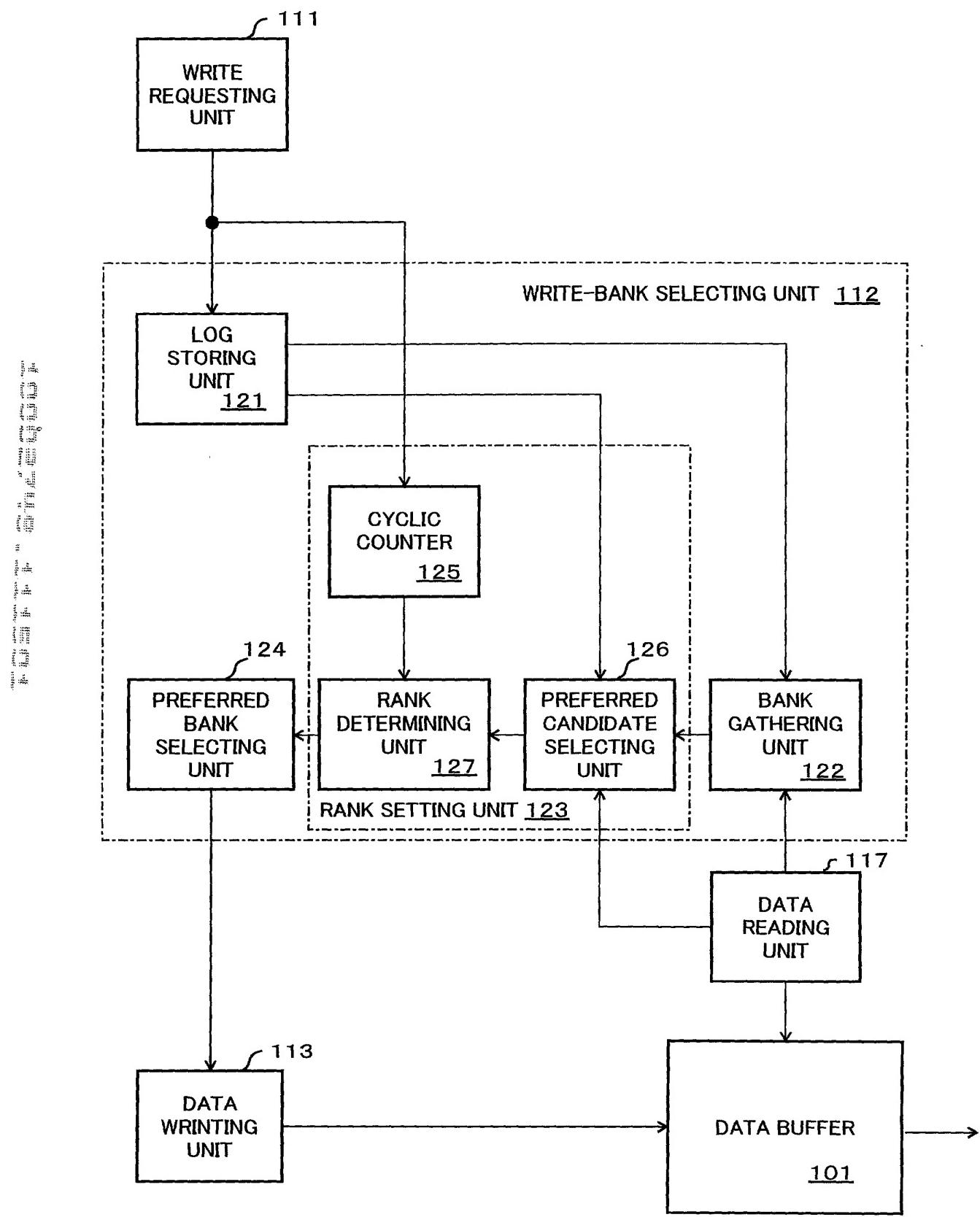


Fig.3

WRITE COMMAND

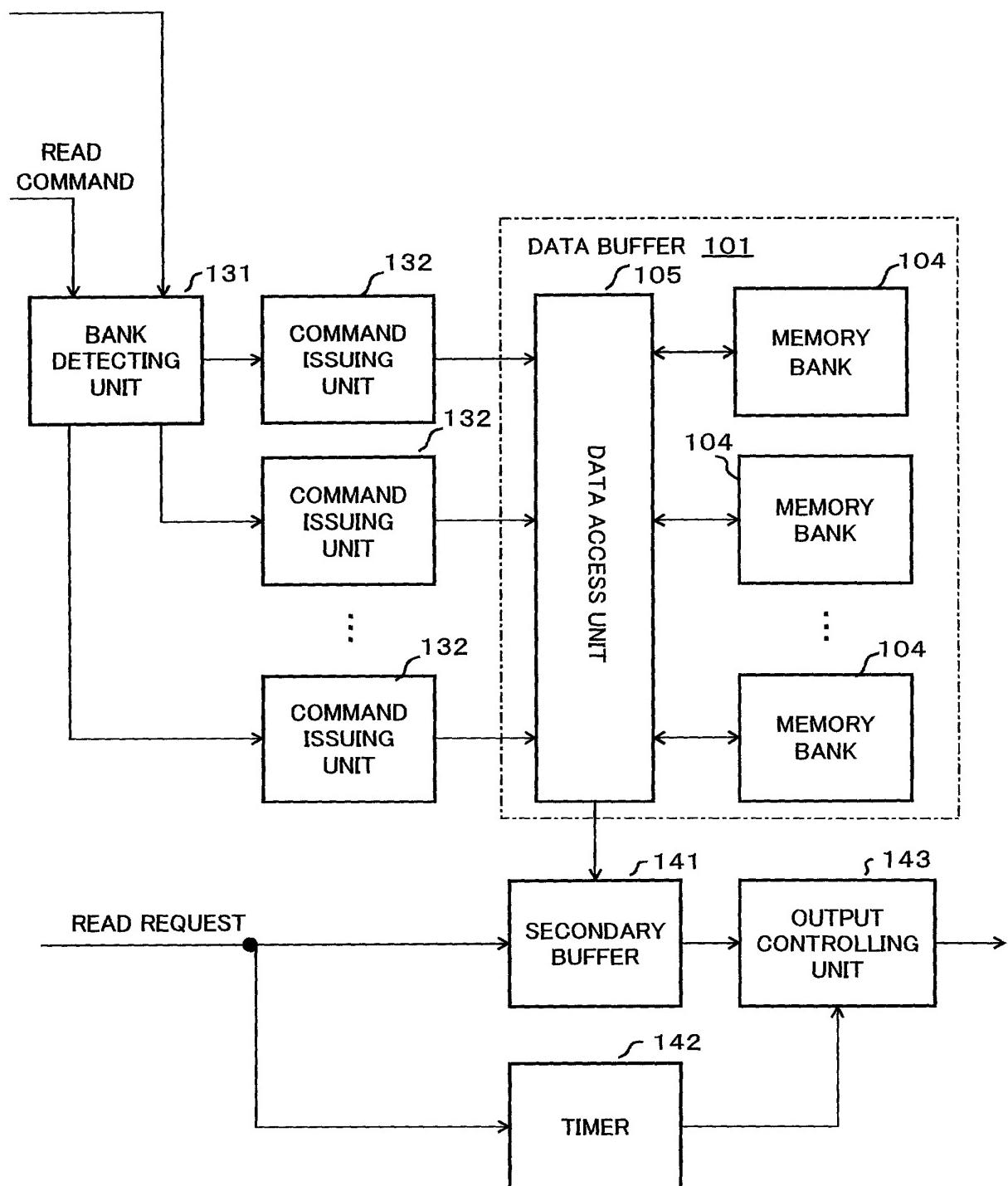


Fig.4

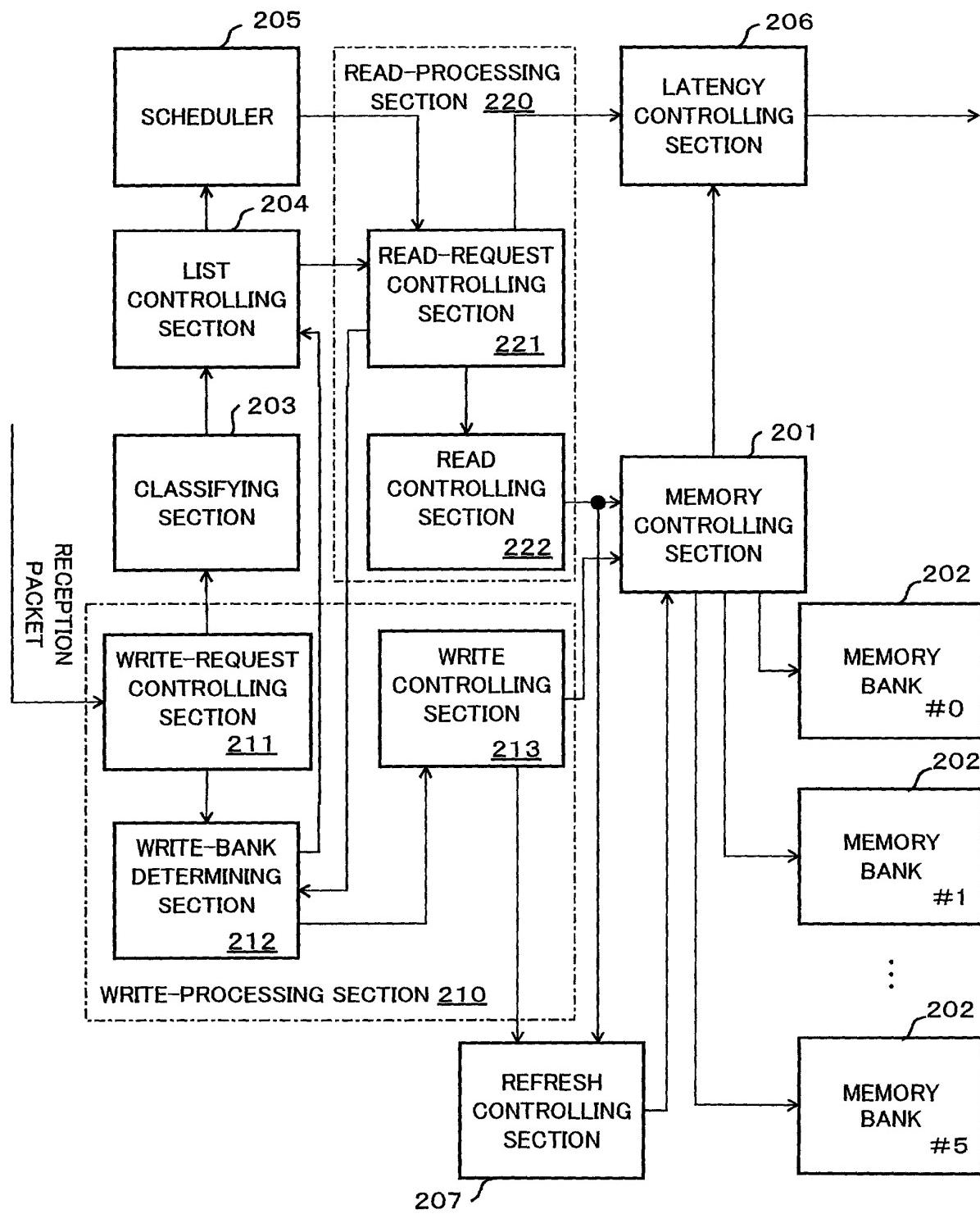


Fig.5

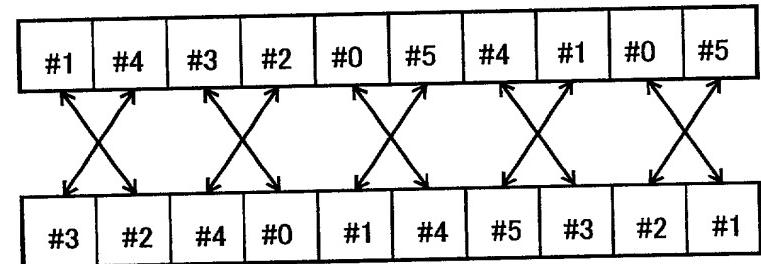
TRANSMISSION PACKETS

S	R	Q
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DATA BLOCKS TO BE READ

S-4	S-3	S-2	S-1	R-4	R-3	R-2	R-1	Q-2	Q-1
(5)	(4)	(3)	(2)	(1)					

CURRENTLY READ BANKS



MEMORY BANKS ASSIGNED AS WRITE BANKS

DATA BLOCKS TO BE WRITTEN

D-2	D-1	C-3	C-2	C-1	B-3	B-2	B-1	A-2	A-1
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RECEPTION PACKETS

D	C	B	A
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MEMORY BANKS
(PERIOD 0)

	R-4	Q-2	#0
	S-4	R-1	#1
	T-1	S-1	#2
	T-2	S-2	#3
T-3	S-3	R-2	#4
T-4	R-3	Q-1	#5

MEMORY BANKS
(PERIOD 1)

		C-2	#0
		C-1	A-1
D-1	A-2	T-1	#2
D-2	B-1	T-2	#3
C-3	B-3	T-3	#4
	B-2	T-4	#5

Fig.6

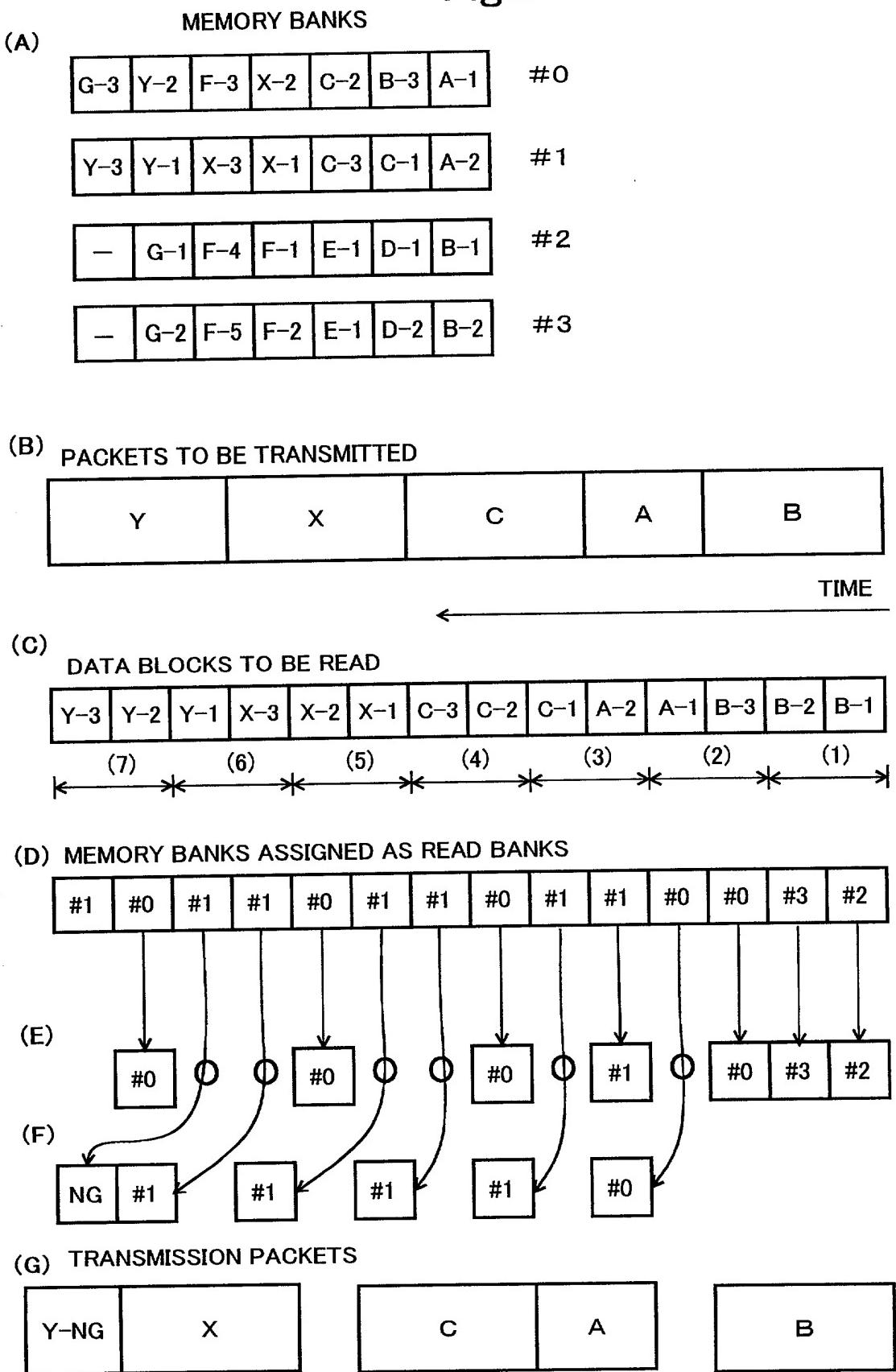


Fig. 7

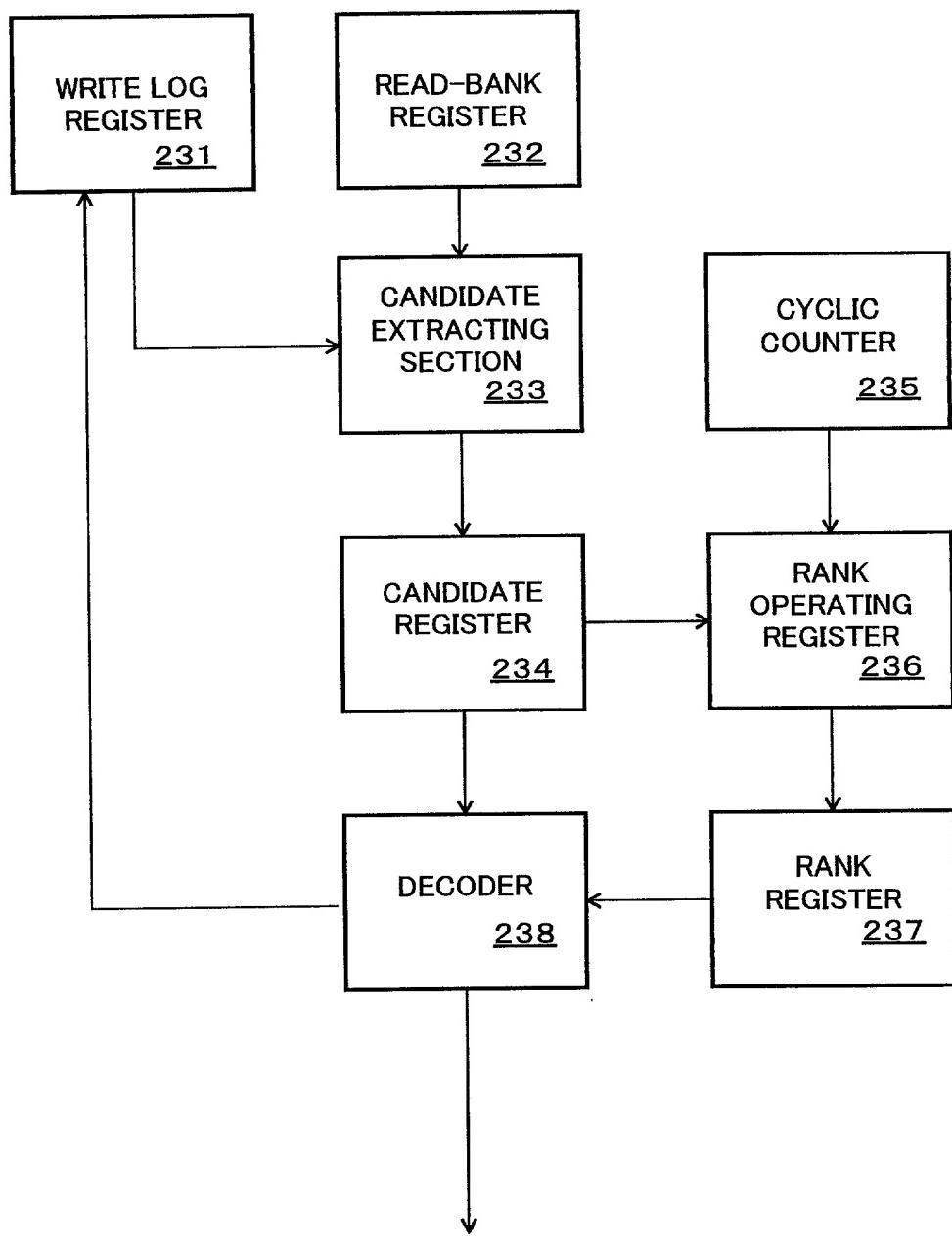
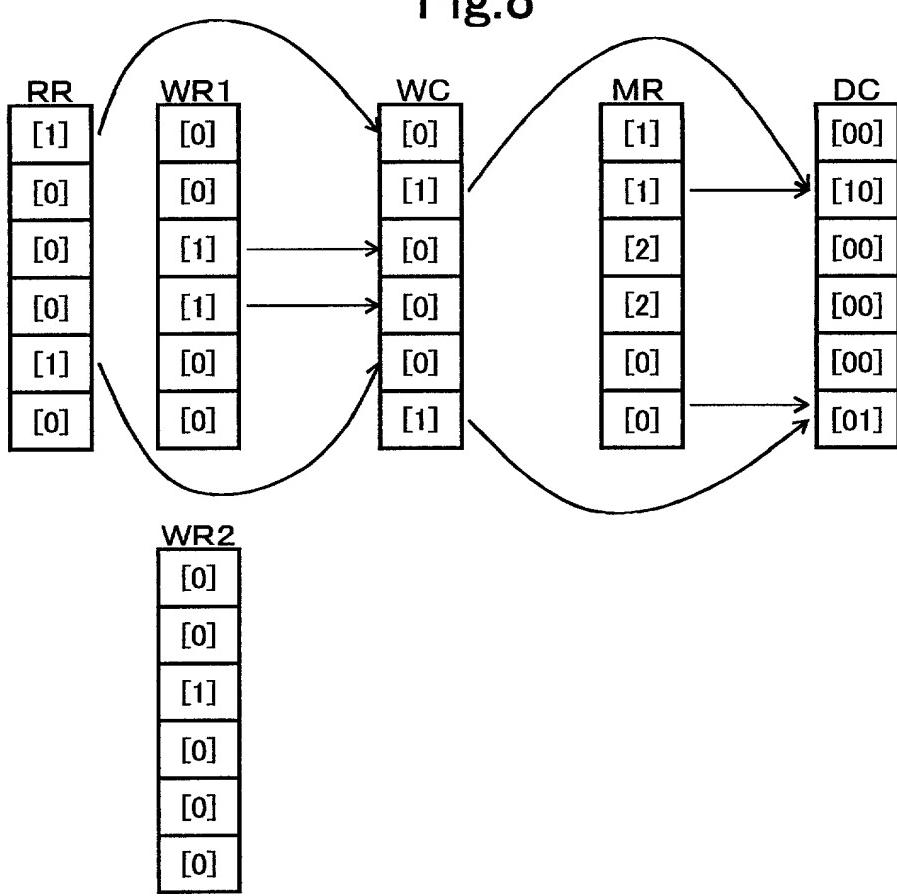


Fig.8

(A)



(B)

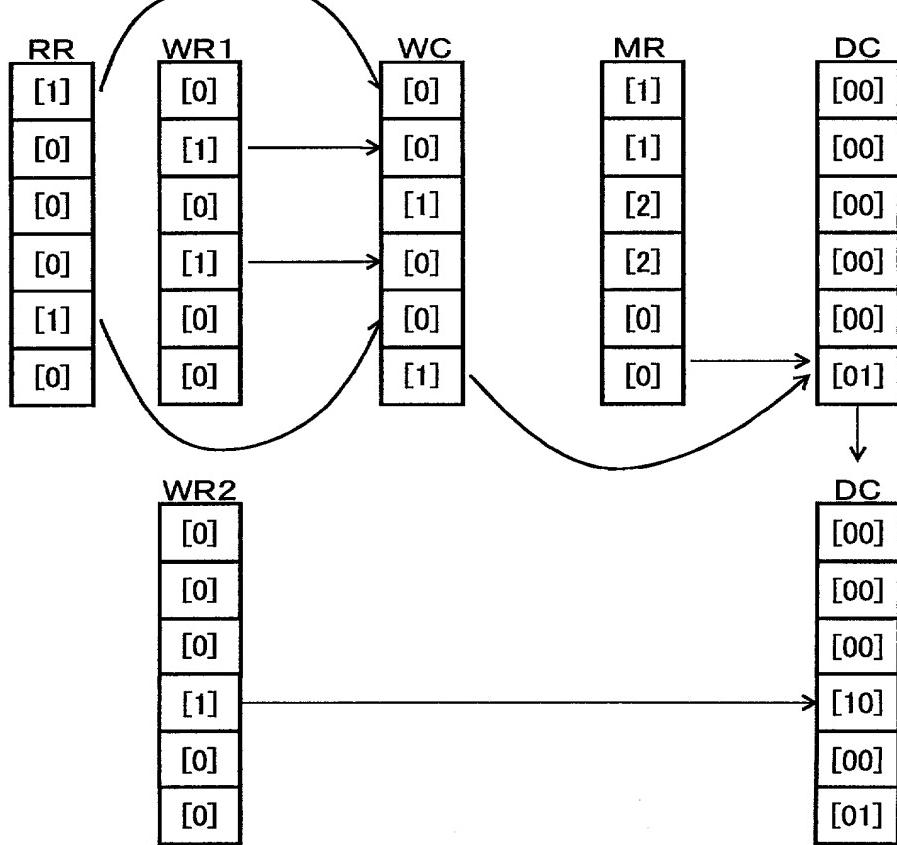


Fig.9

	WC	P0	P1	P2	P3	P4	P5
#0	[0]	0 0	$\Sigma 1-5$ 2	$\Sigma 2-5$ 1	$\Sigma 3-5$ 1	$\Sigma 4-5$ 1	$\Sigma 5$ 1
#1	[1]	$\Sigma 0$ 0	0 0	$\Sigma 2-0$ 1	$\Sigma 3-0$ 1	$\Sigma 4-0$ 1	$\Sigma 5-0$ 1
#2	[0]	$\Sigma 0-1$ 1	$\Sigma 1$ 1	0 0	$\Sigma 3-1$ 2	$\Sigma 4-1$ 2	$\Sigma 5-1$ 2
#3	[0]	$\Sigma 0-2$ 1	$\Sigma 1-2$ 1	$\Sigma 2$ 0	0 0	$\Sigma 4-2$ 2	$\Sigma 5-2$ 2
#4	[0]	$\Sigma 0-3$ 1	$\Sigma 1-3$ 1	$\Sigma 2-3$ 0	$\Sigma 3$ 0	0 0	$\Sigma 5-3$ 2
#5	[1]	$\Sigma 0-4$ 1	$\Sigma 1-4$ 1	$\Sigma 2-4$ 0	$\Sigma 3-4$ 0	$\Sigma 4$ 0	0 0

Fig.10

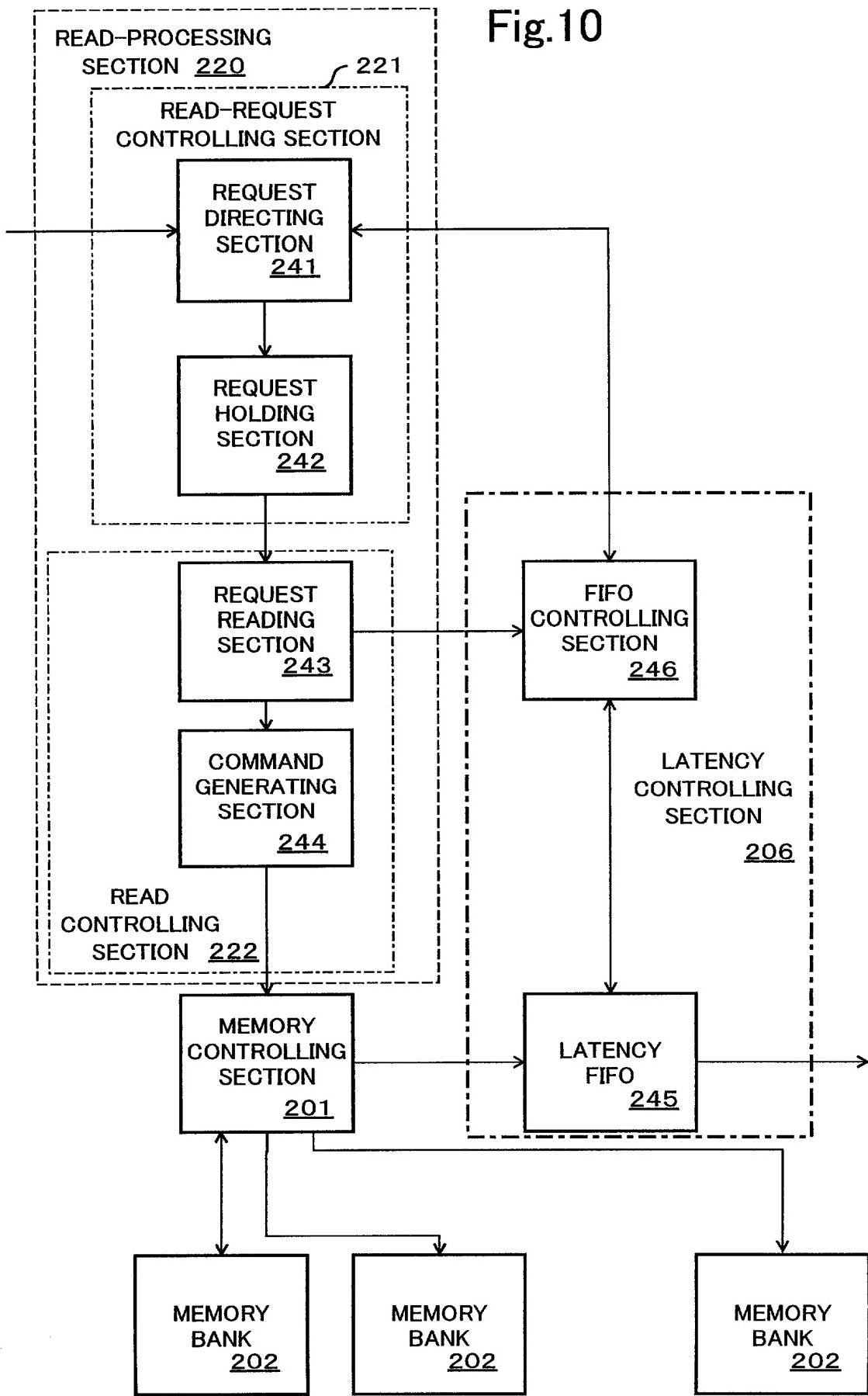


Fig.11

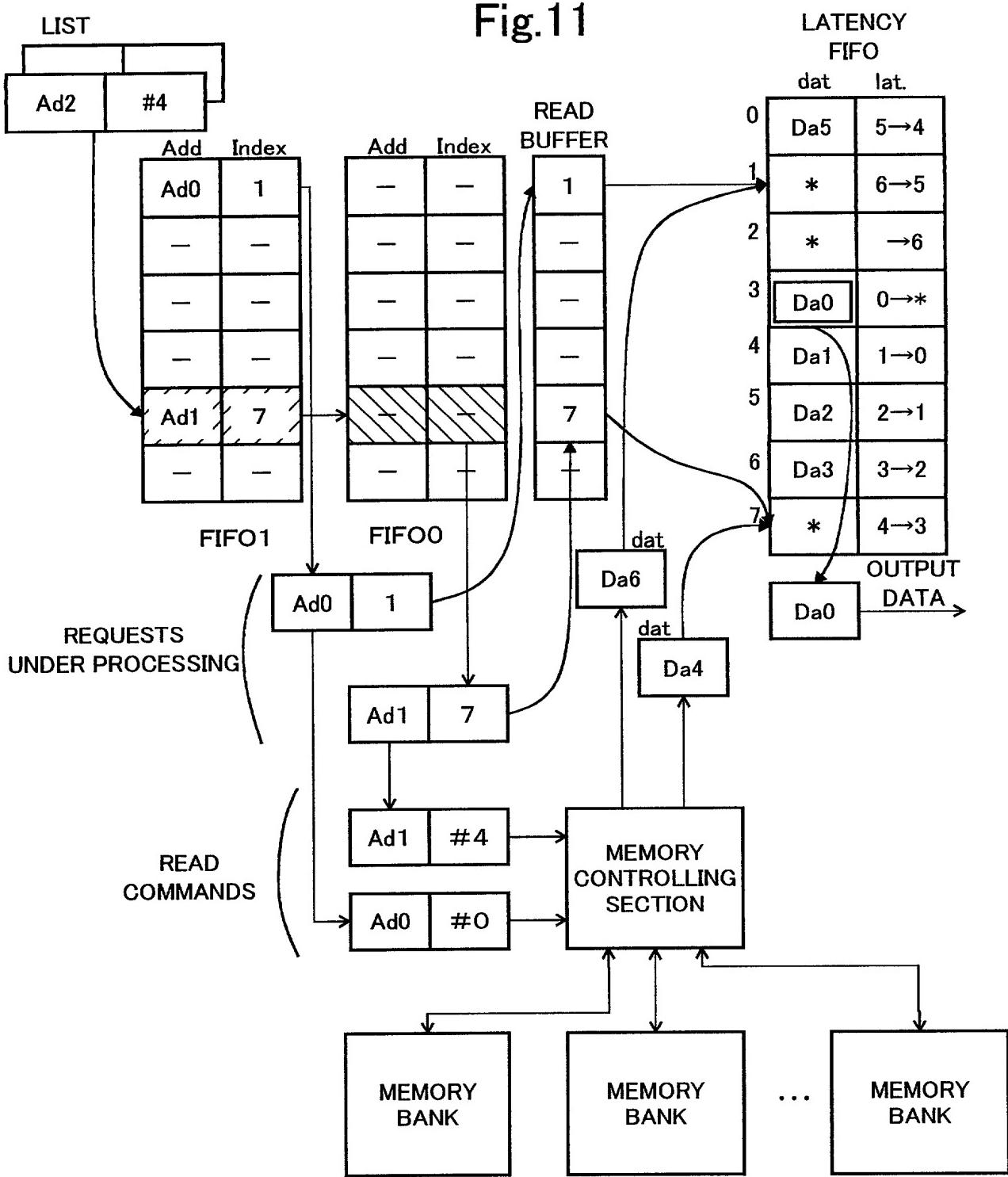


Fig.12

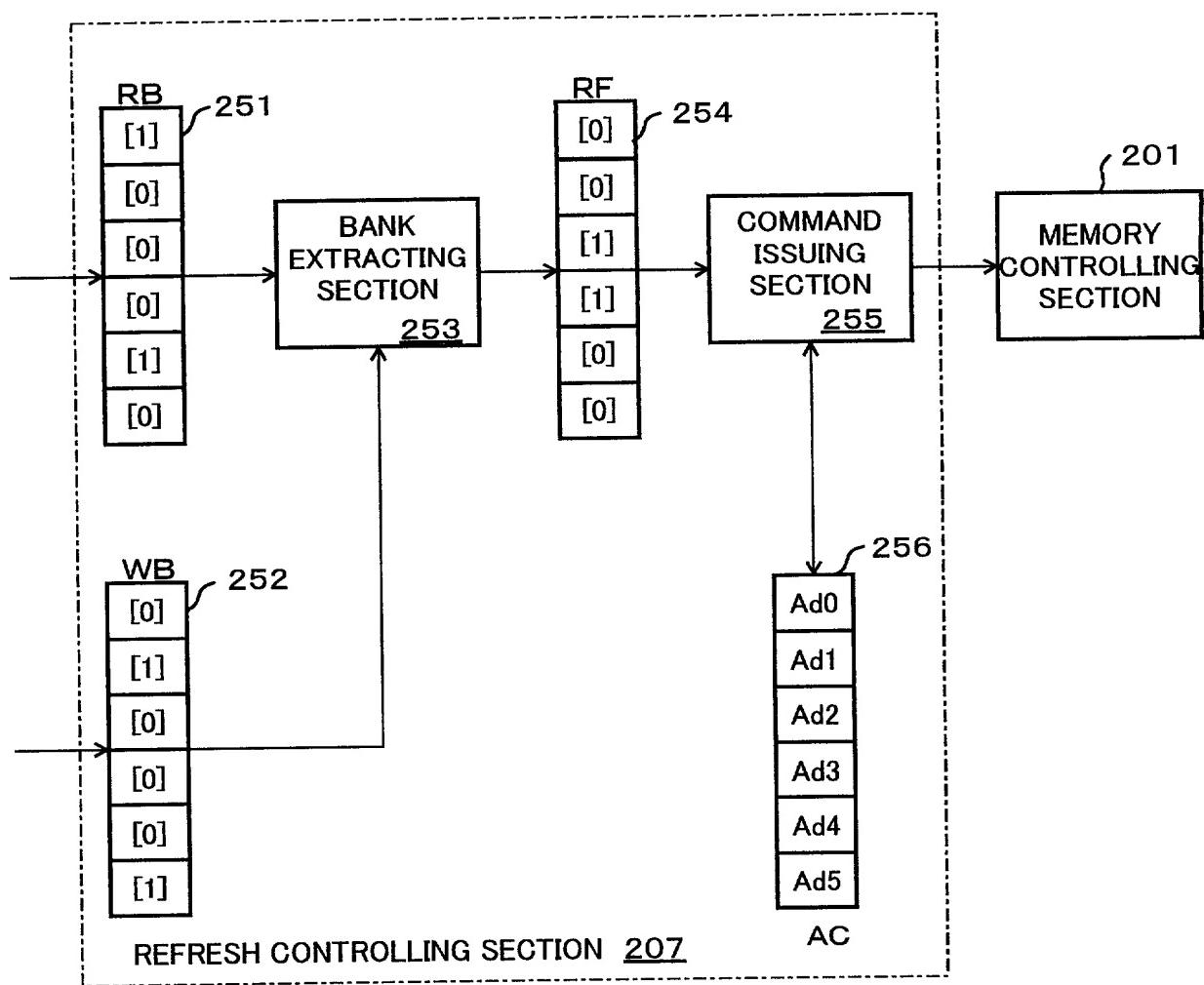


Fig.13 PRIOR ART

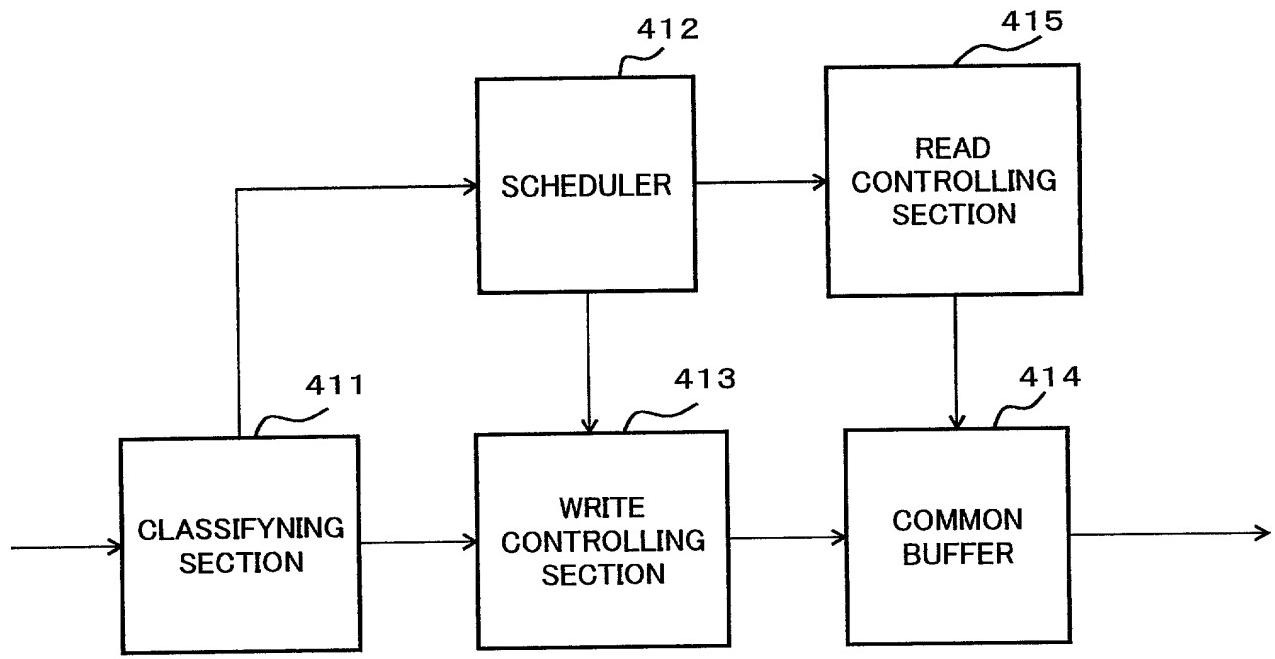


Fig.14 PRIOR ART

